Performances of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger

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Abstract

The ATLAS Barrel Level-1 muon trigger handles data coming from the Resistive Plate Chamber detectors, structured in three concentric layers inside the air-core barrel toroid. The trigger classifies muons within different programmable transverse momentum thresholds, and tags the identified tracks with the corresponding bunch crossing number. The algorithm looks for hit coincidences within different detector layers inside the programmed geometrical road which defines the transverse momentum cut. The Coincidence Matrix ASIC implements the trigger algorithm and the readout of the RPC detector, processing hit signals coming from up to four detector layers. It finds muon track candidates and generates the output trigger patterns with a latency of a few 25 ns bunch crossing periods, and produces and time tags the readout hit patterns. Due to the different performance needs and limitations in the maximum power dissipation and technology, the CMA input pipeline and trigger logic and the time interpolator run at the working frequency of 320 MHz, the readout part works at 160 MHz while the control part works at 40 MHz. Performances of the ASIC have been studied on different test station, the test results are presented.

I. The ATLAS Barrel Level-1 Muon Trigger and the Coincidence Matrix ASIC

The ATLAS level-1 muon trigger makes use of the Resistive Plate Chamber detectors, using the full granularity of the two external stations inside the air-core barrel toroid. The trigger system has to classify muons using six different programmable transverse momentum thresholds, and to tag the muon candidate to the corresponding bunch crossing number. The system provides both trigger and RPC readout information, tagging RPC and trigger hits to time bins of 1/8 of a bunch crossing, 3.125 ns. The algorithm looks for hit coincidences within different RPC detector layers inside the programmed geometrical road which defines the transverse momentum cut. The coincidence is performed on both eta and phi projections.

The on-detector electronics is made of 832 front-end receiver and fan-out boxes (Splitters), 416 low-pt and 416 high-pt trigger processors (PADs). PAD boxes and Splitter boxes are mounted on top of the RPC detectors, connected to the front-end electronics. The off-detector electronics is composed by 64 Sector Logic/RX modules, 64 Interface to MUCTPI boards, 416 Optical links, 32 RODs and 32 ROD backplanes. The trigger slice is composed by one low-pt PAD box, one high-pt PAD box, one Sector Logic board, one MUCTPI interface board, one ROD board.

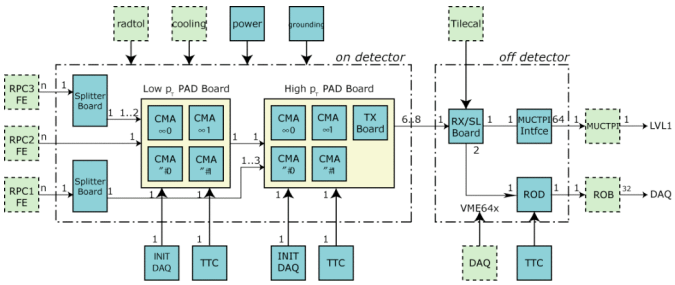

Figure 1: Level-1 Trigger Slice

Figure 1 shows the schematic view of the trigger slice. Signals coming from the RPC front end electronics go to the Splitter boxes, which fan-out signals to the PAD boxes. Low-pt PAD box data are sent to the high-pt PAD, which transmit both low and high-pt results off detector.

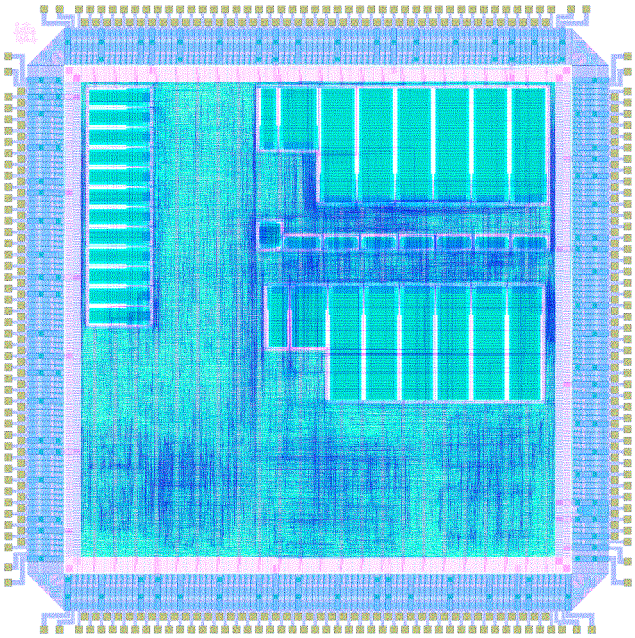

Figure 2: Coincidence Matrix ASIC layout

Each PAD box hosts four Coincidence Matrix ASICs, which implement the trigger algorithm and the readout of the RPC detector on the bending and non-bending views. The CMA processes hit signals coming from up to four detector layers (192 channels) adjusting the time of arrival of hits with

programmable delay lines, in steps of 3.125ns and for a maximum delay of 16 bunch crossing; it finds muon track candidates and generates the output trigger patterns with a latency of a few 25 ns bunch crossing periods (minimum of 3 BCs, depending on the input delay lines setting); it produces and time tags the readout hit patterns, sending data fragments via an 80 Mb/s serial link. The CMA input pipeline and trigger logic and the time interpolator run at the working frequency of 320 MHz. Recovery against SEU is foreseen on all most important configuration registers. This is achieved by designing all relevant internal registers in a 2/3 majority scheme, with the continuous rewriting of the output value on the three sets of registers. Figure 3 and Figure 3 show respectively the ASIC layout and its block diagram scheme.

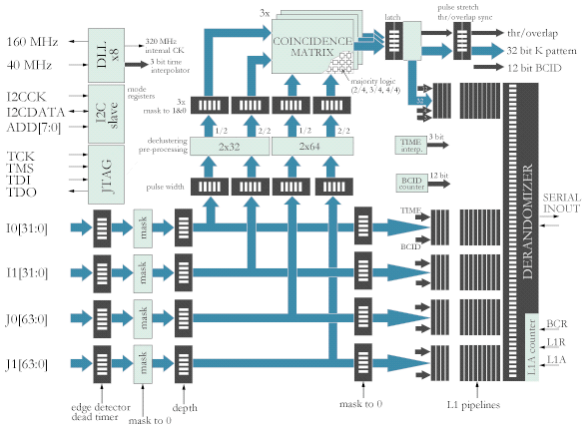

Figure 3: ASIC block diagram

Input pipelines are used to delay and adjust in time input signals, which then go to the trigger logic and to the readout logic. In the trigger logic signals are first masked, de-clustered and pre-processed, and then sent to the three coincidence logic blocks. The readout logic contains latency and de-randomizing memories, level-1 pipeline and time interpolator.

II. Coincidence Matrix ASIC LAB test

The ASIC was submitted during September 2004, and the first batch of industry tested devices was available on March 2005. Test vectors have been automatically generated for the 32 internal logic scan chains (max length 900 FF, 832 patterns, 97% coverage, no scan on timing block and JTAG), while test-bench vectors have been manually generated for the RAM specific scan chain. Finally functional test vectors have been generated for PLL lock test. All these test vectors were used by the industry for low frequency tests (40 MHz). Then functional tests were performed at our lab in Rome.

The ATLAS standard timing and trigger modules were used for lab setup: TTCvi and TTCvx, TTCrq on PADs, 6 test pulse fan-out boards and one splitter board, low and high-pt PADs equipped with 4 CM ASICs each, nine metres long low-to-high pt cable, optical fibre to sector logic. For the initialization and acquisition software, we used the ATLAS DAQ system and a standalone initialization program. Test-pulse and fan-out board were used to distribute signals to all PADs inputs. A standard test-pulse system was used to generate hit signals from the low-pt PAD, using TTC broadcast commands. Level-1 Accept signals were sent every orbit, with busy logic active on PAD or Receiver Sector Logic board.

Data fragment integrity was first checked on all 8 CM ASICs of trigger and readout slice. No corrupted fragments, no BCID errors (periodic BC reset) and no LVL1ID errors were found on 500 kevents. Then timing measurements followed, using 40 ns width input signals to feed the low-pt PAD. Time alignment and shaping of input signals using internal delay line was checked and used for signal alignment during data acquisition. An acquisition window of eight BCs was used. K trigger output pattern was also checked.

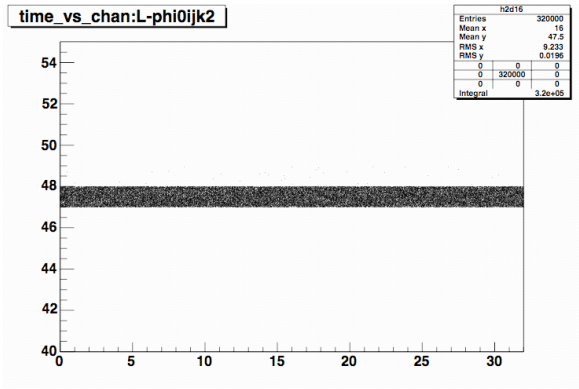

Figure 4: time measurement vs. PAD input channel, Y axis time unit is 1/8 BC, X axis unit is the strip number

Figure 4 shows time measurements versus channel ID for one non pivot layer input on the low-pt PAD, sending the same signal on all input channels. Time is measured in steps of 1/8 of BC, the X axis represents the input channel number (from 0 to 31), the Y axis shows the time slot measured by the ASIC. Figure 5 shows the signals used for this measurement, respectively from top to bottom the 40 MHz input clock, the 40 ns non-pivot and pivot input signals, and the trigger output signal. The non-pivot and pivot inputs were aligned in time by delaying the non-pivot signal, the time difference between trigger output and pivot input is the effective processing and synchronization time of the ASIC.

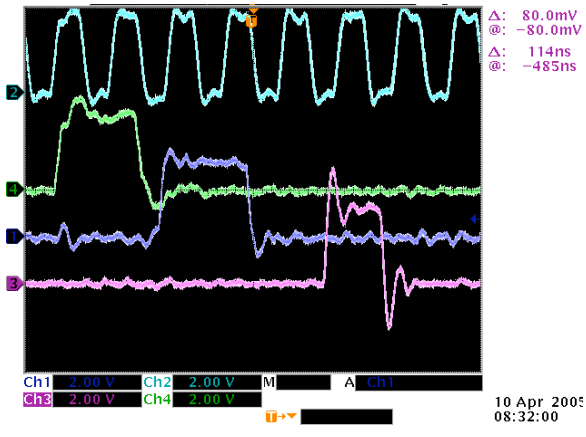

Figure 5: scope view of PAD input and output signals, respectively from top to bottom: the 40 MHz input clock, the 40 ns non-pivot and pivot input signals, and the trigger output signal

The low-pt PAD to high-pt PAD connections were then checked. The final nine meters cable was used to connect the two boxes (differential signals in LVDS standard). The acquisition window on high-pt was shifted by 2 BCs, in order to take into account cable delays. A good correlation on the time measurements obtained by two different ASICs respectively on low and high-pt PADs was observed.

The readout slice was then triggered with an exponential 100 kHz signal generated by the TTC system, simulating the maximum level-1 trigger frequency expected in ATLAS. Synchronization of data measured by delivering test-pulse on two ASICs on a specific BC along orbit was checked, looking at the k trigger low-pt output pattern and at the corresponding high-pt input pattern. No L1ID or BCID loss of synchronization was observed, over all eight ASICs belonging to the readout and trigger slice (3.6 Mevents).

ASIC linearity time measurement has been evaluated by delaying the test-pulse signal in steps of 1 ns. Time has been measured averaging over a full input layer (32-channels). Results are shown in Figure 6. The X axis shows the programmed test pulse delay (in ns), while the Y axis shows the time measured (in 1/8 of BC units).

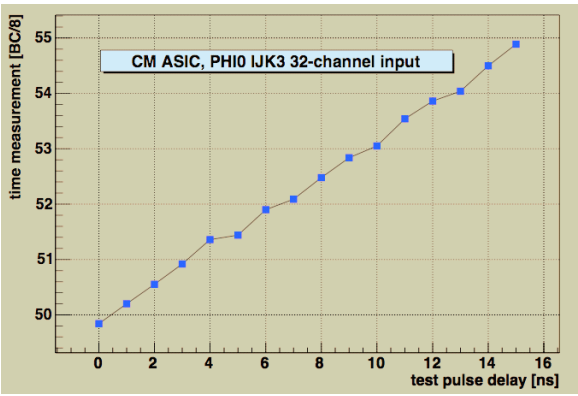

Figure 6: CMA linearity measurement

Finally all possible CMA configurations were tested: control and initialization test (read/write via I2C access on all 190 internal registers); threshold and overlap bits synchronization to 40 MHz TTC clock; full range of pipeline programmable delay; BC reset and BC counter preset logic; L1 reset and L1ID preset logic; input and output masking logic, on both trigger and readout patterns; shaping logic; coincidence algorithm logic (trigger windows, thresholds); all these tests showed the ASIC correct functionality.

III. COSMIC RAY TEST

CERN BB5 cosmic ray test stand, used for MDT-RPC detectors integration test, was used to check the ASIC functionality on a real detector. This test station can host up to three superimposed detectors, packed between the two large RPC detectors making up the cosmic ray hodoscope. Tests were done using trigger electronics for RPC chamber read-out during the few time slots available during the routine certification work. Measures were taken on BMS chambers, later compared with a simple Montecarlo application results.

Timing calibration had to be done in order to be able to align in time readout data, and to perform the proper coincidence between low and high-pt signals. Hit time distribution for each RPC plane was used to extract calibration constants needed for time alignment and for sliding time distribution within the same BC. Figure 7 shows the measured RPC strip geometry, the two axes representing the strip profiles for two eta layers, belonging respectively to one pivot and to one confirm RPC plane. The plot shows a good correlation between different RPC strips planes.

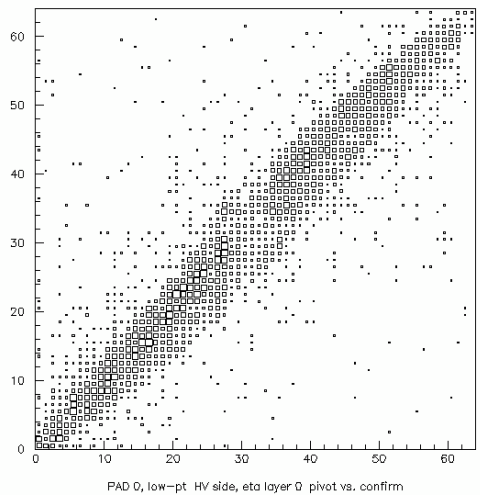

Figure 7: strip geometry, strip profile for two RPC eta layers, pivot vs. confirm planes, both axes unit is strip number

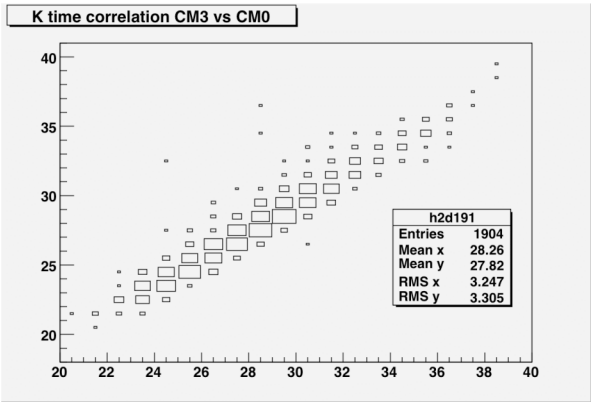

Figure 8: time correlation between two different CMAs, one eta and one phi, inside one PAD, both axes unit is time (1/8 of BC) for the k trigger pattern

Time correlation between different planes was then investigated. Figure 8 shows time correlation between one eta CMA and one phi CMA, both belonging to the same PAD. Both axes show the measured time for the CMA k trigger output patterns, one eta and one phi. Again good correlation between the two patterns was observed.

Trigger tower efficiency was then measured, varying both the RPC detector HV values and the front-end threshold voltage. Trigger efficiency on one trigger tower was compared to the Montecarlo expected values (data: 3/4 majority, full roads, MC: 100% efficiency). Good correlation

was observed between the measured values and the Montecarlo calculated values. Figure 9 shows the fraction of measured muons within one trigger tower as a function of the detector HV value. Figure 10 shows the measured trigger rate as a function of the front-end electronics threshold voltage. In both plots the maximum efficiency point is comparable with the corresponding Montecarlo predicted value.

Trigger rates were then measured in self-trigger mode, in order to verify both detector and electronics stability. Measured rates were again compared with the foreseen Montecarlo values. The MC toy foresees about 290 Hz trigger rate for an ideal detector, while with a majority of 3/4, full trigger acceptance, we measured about 280 Hz on both trigger towers of a single chamber.

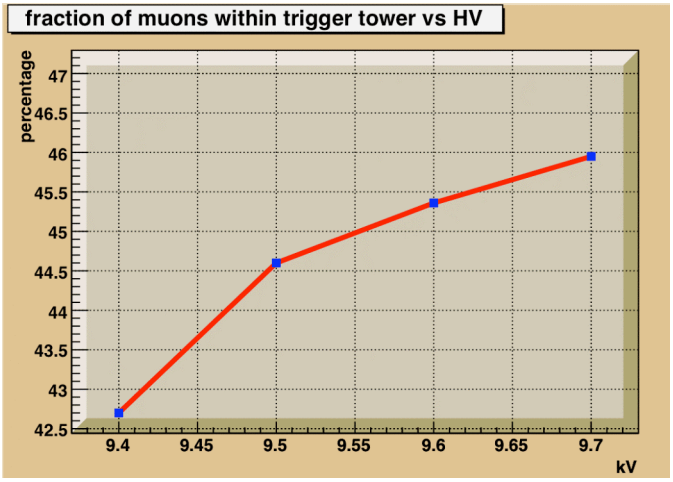

Figure 9: fraction of the measured muons within the trigger tower versus high voltage value

All the required ASICs have been now produced. 4800 devices (4 wafers) were delivered in August. Two wafers are still in foundry under nitrogen flux as spares. ASIC industrial test was concluded in September. The measured yields are:

- room temperature yield = 82.7%;
- high temperature yield = 98.9% (on room temperature tested sample);
- final total yield = 81.8 %.

4200 packaged ASIC are now available (3320 needed for ATLAS start-up) for being mounted on CM mezzanines.

IV. Conclusions

All ASICs have passed the production test with test vectors after packaging, plus the X-ray + JTAG boundary scan after being mounted on CM mezzanines. Functional lab test using test-pulses are foreseen after PAD boxes assembling.

CMA technology (UMC 0.18 μm) was already tested against radiation on a proton beam at Louvain-La-Neuve, and successfully passed our radiation selection criteria. Qualification test on final full integrated boards is foreseen.

Cosmic ray test measurements are preliminary studies, to be used as a starting point for the commissioning work. Trigger electronics is now being mounted on one ATLAS trigger sector, to be used for the commissioning phase.

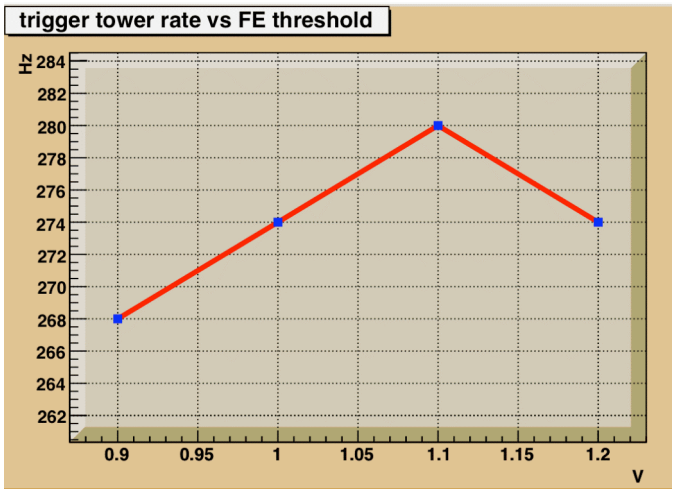

Figure 10: measured trigger rate for the trigger tower versus front-end threshold voltage

V. References

[1] V. Bocci, G. Chiodi, S. Di Marco, E. Gennari, E. Petrolo, A. Salamon,, R. Vari, S. Veneziano, "Prototype Slice of the Level-1 Muon Trigger in the Barrel Region of the ATLAS Experiment", in Proc. LECC 2001 pp. 236-239.

[2] E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "Barrel LVL1 Muon Trigger Coincidence Matrix ASIC User Requirement Document", ATL-COM-DAQ-2000-050.

[3] E. Petrolo, A. Salamon, R. Vari, S. Veneziano "CMA ASIC Hardware Requirement document", ATL-COM-DAQ-2001-005.

[4] E. Gennari, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "Radiation Tolerance Evaluation of the ATLAS RPC Coincidence Matrix Submicron Technology", in Proc. LEB 2000, 2000, pp. 236-239.

[5] V. Bocci, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "The Design of the Coincidence Matrix ASIC of the ATLAS Barrel Level-1 Muon Trigger", in Proc. LECC 2002, pp. 261-265.

[6] V. Bocci, E. Petrolo, A. Salamon, R. Vari, S. Veneziano, "The Coincidence Matrix ASIC of the Level-1 Muon Barrel Trigger of the ATLAS Experiment", in IEEE TNS, Aug. 2003, vol. 50, no 4.

[7] G. Aielli et al., "Slice Test Results of the ATLAS Barrel Muon Level-1 Trigger", in Proc. LECC 2003.

[8] G. Aielli et al., "Test Beam results and integration of the ATLAS Level-1 Muon Barrel Trigger", in Proc. NSS-MIC2004.